



Image
2814
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Application of:

Baluswamy et al.

Serial No.: 09/996,337

Filed: November 28, 2001

For: RAISED-LINES OVERLAY
SEMICONDUCTOR TARGETS AND
METHOD OF MAKING THE SAME

Examiner: M. Pizarro Crespo

Group Art Unit: 2814

Attorney Docket No.: 2269-4307.1US
(99-1193.01/US)

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

November 24, 2003

Date

Signature

Deidra Pfeil

Name (Type/Print)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. The listed document is from co-pending application Serial No. 09/651,790, filed August 30, 2000. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

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In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Publication Date</u>	<u>Patentee</u>
5,883,012	03/1999	Chiou et al.

Other Documents

Ghandhi, "VLSI Fabrication Principles Silicon and Gallium Arsenide", 2nd ed., 1994, John Wiley & Sons, Inc., New York, pp. 589

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is filed after the mailing date of the final Office Action under 37 C.F.R. § 1.113, but before payment of the issue fee.

I hereby certify that no item of information contained in the Supplemental Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the statement. Pursuant to 37 C.F.R. § 1.97(d)(ii), applicant hereby requests

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consideration of the accompanying Supplemental Information Disclosure Statement. The fee pursuant to 37 C.F.R. §1.17(p) for consideration of this Supplemental Information Disclosure Statement is enclosed.

Respectfully submitted,



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Date: November 24, 2003
JRD/sls:djp

Enclosures: Form PTO-1449 or PTO/SB/08
Copy of documents cited
Check No. 5369 in the amount of \$180.00

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